REMARKS

The indication of allowable subject matter in claim 3 is acknowledged and appreciated. Accordingly, claim 14 has been added which corresponds to claim 3 rewritten into independent form. In view of the following remarks, it is respectfully submitted that all claims are in condition for allowance.

Claim 1 is the sole rejected independent claim and stands rejected under 35 U.S.C. § 103 as being unpatentable over Asami '100 ("Asami") in view of Dreifus '621 ("Dreifus"). This rejection is respectfully traversed for at least the following reasons.

Claim 1 recites in pertinent part, "state control means for halting operations of said CPU while said transmission circuit is sending/receiving data to/from the outside" (claim 13 is submitted to be patentable for at least reasons similar to those that will be discussed below with respect to claim 1). That is, the CPU can be in a halt state while data is transmitted by the transmission circuit. The Examiner relies on control circuit 8 of Asami as both the CPU and the state control means. However, for at least the following reasons, it is respectfully submitted that the control circuit 8 of Asami is not a state control means which halts the operations of the CPU.

Turning to the device of Asami, while data is received from host system apparatus 2 by the Trans/Receipt antenna unit 3, the alleged control circuit 8 executes a particular error detection processing for the received data and temporarily stores the data at buffer 10 (*see* col. 5, lines 1-9). Accordingly, the alleged control circuit 8 is not in the halt state while data is transmitted to the Trans/Receipt antenna unit 3. Instead, the alleged control circuit 8 disables writing operations to memory 7 but is nonetheless still in the operative state.

In particular, the alleged control circuit 8 of Asami executes writing operations on the buffer memory while the alleged transmission circuit is sending/receiving data from the host

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system apparatus (*see* col. 5, lines 1-9); whereas as embodied by claim 1 of the present invention, the CPU does not execute write/read processing on the buffer memory while the transmission circuit is sending/receiving data from the outside because the state control means can halt the operations of the CPU. Instead, the DMA circuit can execute write/read processing on the buffer memory. Accordingly, Asami fails to disclose or suggest, *inter alia*, a "state control means for halting the operations of said CPU."

Dreifus, on the other hand, discloses only a DMA circuit that is connected to the RAM. Dreifus is completely silent as to a "state control means for halting the operations of said CPU." Indeed, the Examiner does not rely on Dreifus for such a feature and instead relies exclusively on Asami for allegedly disclosing the claimed state control means.

In conventional contactless IC cards, the power supply is less stable so the data may not be normally received/sent due to the influence of noise caused by the operation of the CPU. Accordingly, one object of the present invention is to provide an IC card capable of suppressing the influence of noise and one means by which to do so includes providing a state control means, which can halt the operation of the CPU, along with the other elements recited in the novel ***combination*** of elements recited in claim 1.

In view of the foregoing, it is respectfully submitted that neither Asami nor Dreifus, alone or in combination, disclose or suggest a "state control means for halting the operations of said CPU", let alone in the particular combination of elements recited in claim 1. The Examiner is directed to MPEP § 2143.03 under the section entitled "All Claim Limitations Must Be Taught or Suggested", which sets forth the applicable standard:

> To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (citing *In re Royka*, 180 USPQ 580 (CCPA 1974)).

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In the instant case, the pending rejection docs not "establish *prima facie* obviousness of [the] claimed invention" as recited in claim 1 because the proposed combination fails the "all the claim limitations" standard required under § 103.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 1 is patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

For example, referring to claim 10, a DMA circuit can transmit data when the CPU is in a halt state. Turning to the cited prior art, Asami does not disclose a DMA circuit and Dreifus discloses only a DMA circuit that is connected to the RAM. Both Asami and Dreifus are completely silent as to when a DMA circuit can transmit data.

As yet another example, referring to claim 11, a state control means can be in an operative state when the CPU is in a halt state. The Examiner alleges that the control circuit 8 of Asami is read as both the state control means and the CPU. As a result of this interpretation, there is created an inherent inconsistency because the control circuit 8 can not be in an operative state when the same control circuit 8 is in a halt state.

As still yet another example, referring to claim 12, a state control means can give an active state control signal whereby the CPU is restored to the operative state from the halt sate, when the transmission circuit completes the send/receive operation. The Examiner alleges that the control circuit 8 is read as both the state control means and the CPU. As a result of this

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interpretation, there is created an inherent inconsistency because the control circuit 8 is only a single element.

Based on all the foregoing, it is submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejections under 35 U.S.C. § 103 be withdrawn.

CONCLUSION

Having fully and completely responded to the Office Action, Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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